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54) Circuit arrangement for supplying a fan-out current for a data driver unit.

57) A circuit arrangement is presented for supplying a specified fan-out current for a data driver unit (DT) operating on a transmission line (L). In this case the fan-out current flows through a plurality of partial current paths which are switched in parallel, and of which as many are connected through by a control circuit (ST) as required for the total current to represent the desired fan-out current. The control circuit itself is controlled by a comparator (K), which compares the fan-out current of the data driver unit or an equivalent reference data driver unit (RT) with a reference voltage ($U_R$) and makes the control circuit switch on or switch off partial current paths when the fan-out current of the data driver unit deviates from the reference voltage.

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The invention relates to a circuit arrangement according to the preamble of claim 1.

In order to transmit unadulterated wide band signals over a line it is necessary to precisely adjust the output impedance of the transmitter and the input impedance of the receiver to the characteristic impedance of the transmission line. This becomes difficult, especially when integrated circuits whose impedances can not be efficiently adjusted during production to within a few percent of a specified value are used as the transmitters or receivers.

In order to preserve a precise impedance value despite this, one can produce a circuit with a very high output or input impedance and hook up to it an external resistance element. The external resistance element can be relatively easily adjusted, such that the total impedance corresponds to the required impedance.

The high resistivity of such a circuit, in particular when adapting the outputs, causes a high degree of dependance of the output level as well as all levels on the line being driven on the fan-out current. Consequently, the last one has to be adjusted as precisely as possible and held constant.

However, as a rule, the nominal fan-out currents of integrated circuits vary due to process fluctuations and due to temperature and supply voltage variations within a range which can attain ± 20% in bipolar systems, and over ± 50% in CMOS systems. This leads to unacceptable fluctuations of signal levels on the driven line.

Because of this, attempts have already been made to regulate the output impedances of the output circuits continuously. Such a circuit is know, for example, from a paper by Knight and Krymm in IEEE Journal of solid-state circuits, vol. 23, No. 2, April 1988. However, for regulation purposes, this circuit requires analog components such as, for example, linear amplifiers (Fig. 9), which render them useless for wide band signals with more than 50 MBit/s. Besides this, in this case one employs as current sources low-resistance switches which are connected to integrated, adjustable series resistances.

The object of the invention is to present a circuit arrangement, which permits to adjust the fan-out current without analog circuits, and is suitable for wide band signals up to 150 MBit/s.

A circuit arrangement which accomplishes this task is described by the characteristics of claim 1. The parallel switching of various current paths, which form equal or different staggered parallel output resistances, allow to adjust the total output resistance digitally using only switches.

Further details of circuit arrangement according to the invention are presented in the sub-claims.

Thus, claims 2 and 3 relate to the magnitudes of the parallel output resistances. Claim 4 provides for the regulation of servo components of several data driver units by a single control circuit. In doing this according to an embodiment of the circuit arrangement according to invention described in claim 5 this single control circuit can be assigned to a reference data driver unit, which is not used for data transmission, but, instead, operates on a transmission line at a previously specified reference resistance.

The object of claim 6 is a measure for saving energy. It also prevents a heating up of the reference impedance and a potential change of the impedance value associated with this heating.

Finally, claims 7 and 8 relate to embodiments of the control circuit which steer the servo components of one or more data driver units.

Example embodiments of control circuit according to the invention will now be described in detail, including their functioning, based on the figures.

Fig. 1 shows a block circuit diagram of a multiple data driver unit with a reference driver,
Fig. 2 shows the structure of a data driver unit,
Fig. 3 shows the structure of a control circuit.

Fig. 1 shows a series of data driver units $DT_1$ ... $DT_n$, which pass signals delivered to them through data inputs $D_1$ ... $D_n$ to transmission lines $L_1$ ... $L_n$. The data driver units have defined output impedances, which are adapted to the characteristic impedances of the transmission lines and are constituted by external output resistances (not shown). The required fan-out currents flow through one or several current paths which are switched in

parallel and connected individually by a preparation signal VS issued separately for each current path of a data driver unit from a control circuit.

The preparation signals VS are issued by the control circuit ST depending on the output signal of a comparator K, which compares the output voltage of a reference data driver unit $R_T$ operating with a reference resistance $R_R$ with a previously specified reference voltage $U_R$, and orders the control circuit to connect additional current paths if the output voltage measured on the reference data driver unit drops below the reference voltage. This connection is performed by issuing other or additional preparation signals, which affect all data driver units including the reference data driver unit.

Inside the data driver units the preparation signals are added to the data arriving via the corresponding data inputs, such that the desired nominal currents flow through the external output resistances, and data are sent out to the signal lines with the desired amplitudes.

The structure of a data driver unit is illustrated in Fig. 2. A plurality of current paths, each comprised of two MOS field effect transistors (MOSFETS) $T_{10}$, $T_{20}$, ... $T_{1n}$, $T_{2n}$ switched in series, are connected in parallel with respect to each other and comprise in their totality a partial resistance of a voltage divider. The other partial resistance of this voltage divider is an external work resistor $R_A$ connected to positive voltage +U. At the junction point between the two partial resistances is connected a signal line L.

Of the MOS field effect transistors switched in series the ones shown on the top in the figure, MOSFETS $T_{10}$, ... $T_{1n}$, serve for switching through a stream of digital data supplied through a data input D. MOSFETS $T_{20}$, ... $T_{2n}$, shown on the bottom in the figure, are used for connecting the individual current paths depending on the preparation signals, which are generated by the control circuit, and supplied via the preparation signal lines VS to the gate terminals of these MOSFETS.

Just one MOSFET, $T_{20}$, whose gate is hooked up to positive voltage and whose source is connected to negative voltage -U is switched through at all times.

All MOSFETS also represent load resistances. Their magnitudes are chosen such that the individual current paths conduct specified partial currents. In the data driver unit shown in Fig. 2 the current path illustrated on the right is designed in such a way, that the current flowing through MOSFETS $T_{10}$ and $T_{20}$ remains slightly below the nominal current

flowing through the work resistor. The other current paths are designed in such a way, that in their totality, i.e. switched in parallel, they deliver a supplementary current, which increases the current flowing through the work resistor to a value slightly above the nominal current. In this case, the load resistors of the individual current paths are either equal or graded in such a manner, that their electric conductances are related to each other by powers of a positive number, for example, of the number 2.

In a data driver circuit, such as the one illustrated in Fig. 2, one can also use bipolar transistors instead of MOSFETS. In this case, resistances are added in order to preserve the desired resistance values for the individual current paths. Likewise, it is also possible to use p-channel MOSFETS instead of the n-channel MOSFETS shown in Fig. 2, and it is also possible to construct the data driver units with reversed output polarity.

Fig. 3 illustrates the principle of a control circuit, which is suited for issuing preparation signals for a larger number of, for example, data driver units combined in one integrated circuit.

An up-down counter VRZ counts pulses of a clock TG, which arrive individually each through an AND gate either to an up-counting input VE or a down-counting input RE. The parallel output of the up-down counter is hooked up to a multiplexer MX, from whose outputs are derived the preparation signals VS1, ... VSn. The preparation signals are also supplied to a reference data driver unit RT, which corresponds to the usable data driver units in its construction, but, instead of being connected to a signal line, it operates with a reference resistance $R_R$. In case all of the transistors in this reference driver unit, which are otherwise controlled by the data line, are switched through all the time, then the current flowing through the reference resistance depends on the number and valency of the preparation signals and represents the nominal current.

For continuous control of this nominal current one measures on the reference resistance $R_R$ the voltage drop with respect to the positive voltage +U and compares it with a specified reference voltage $U_R$ in a comparator K. The output of the comparator is connected once directly and once via an inverter with the inputs of the AND gates, which are switched before the two counter inputs.

If the voltage drop recorded across the reference resistance exceeds the reference voltage, then the comparator opens the down-counting input of the counter VRZ.

Consequently, the counter counts down, which leads to switching off of preparation signals and thus to the interruption of current paths in the data driver units. Since the reference data driver unit also receives the preparation signals, the current through the reference resistance $R_R$ drops as well. Consequently, the voltage drop caused by this current falls below the reference voltage $U_R$, which causes a reversing of the down-counting input and opening of the up-counting input of counter VRZ. Thus, the counter again activates additional preparation signal lines.

If one employs a window comparator instead of conventional comparator, then one can easily produce a condition in which the counter does not count up or down. One also has the possibility of only regulating the driver fan-out currents from time to time. In this case the reference driver unit does not need to be operating continuously.

## Claims

1. Circuit arrangement for producing a specified fan-out current, comprising a data driver unit which sends out a data signal on a line and has a comparator for measuring an output voltage and evaluating this output voltage in comparison to a reference voltage, and also has a control circuit, which, depending on the output signal of the comparator, controls a servo component which changes the fan-out current, **characterized in that** the servo component possesses a plurality of parallel switched current paths ($T_{10}$, $T_{20}$, ... $T_{1n}$, $T_{2n}$), each exhibiting a resistive load and capable of being switched on independently of each other, whereby the turning on of a current path is accomplished jointly by a data signal supplied to the data driver unit and a preparation signal of the control circuit (ST) through applying to them an AND function, and in that the preparation signal is issued only to circuit elements of those current paths, whose total sum of pass-through currents corresponds to the specified fan-out current.

2. Circuit arrangement according to claim 1, characterized in that the first one of the parallel current paths exhibits a resistive load whose magnitude is such, that the current flowing through it is smaller than the specified fan-out current by a specified amount, and that the resistive loads of the other parallel current paths are equal amongst each other and have such a magnitude, that the currents flowing through them together with the current flowing through the first parallel current path yield a total current, which is larger than the specified fan-out current by a specified amount.

3. Circuit arrangement according to claim 1, characterized in that the resistive loads of the parallel current paths exhibit such magnitudes, that the currents flowing through them yield a total current which is larger than the specified fan-out current by a specified amount, and that electric conductance values of the resistive loads are related to each other by powers of a positive number, in particular the number 2.

4. Circuit arrangement according to claim 1, 2 or 3, characterized in that the control circuit (ST) uses additional servo components to change the fan-out currents of additional data driver units ($DT_1$, ... $DT_n$) of the same type.

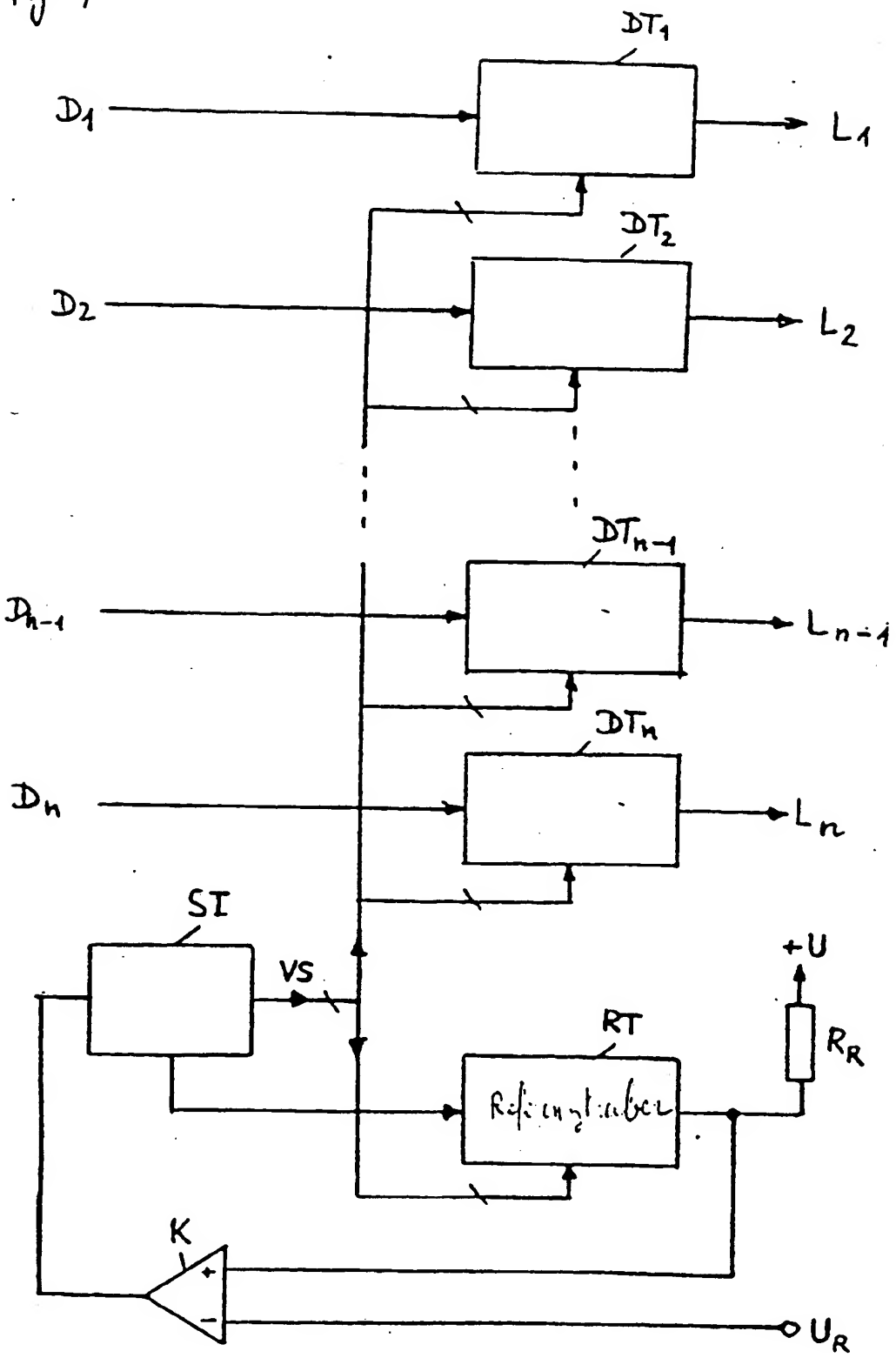
5. Circuit arrangement according to one of the preceding claims, characterized in that a reference data driver unit which operates with a reference resistance and whose structure corresponds to that of a data driver unit is provided, and in that the output voltage of this reference data driver is used as the output voltage for comparison with a reference voltage.

6. Circuit arrangement according to claim 5, characterized in that the reference data driver unit (RT) is only switched on from time to time for a specified duration, and that the control circuit (ST) stores a servo component control signal determined during this time and keeps it memorized until the next switch-on time.

7. Circuit arrangement according to one of the preceding claims, characterized in that the control circuit comprises a counter (VRZ) which counts up or down depending on the comparator output signal, and that when a specified counter status is achieved preparation signals are issued to circuit elements ($T_{1,0}$, ..., $T_{2,n}$) of specified current paths.

8. Circuit arrangement according to claim 7, characterized in that the counter has a binary output, and that the signals appearing at the output bit-lines of this binary output are used as preparation signals for circuit elements ($T_{21}$, ..., $T_{2n}$) of specified parallel current paths, and in that the assignment of current paths to the individual output bit-lines supplying the preparation signals is chosen in such a way, that the electric conductivity of each individual current path is proportional to the valence of the bit-line which delivers the preparation signal for that current path.

Fig 1


DT1
D1
L1
DT2
D2
L2
DTn-1
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Ln-1
DTn
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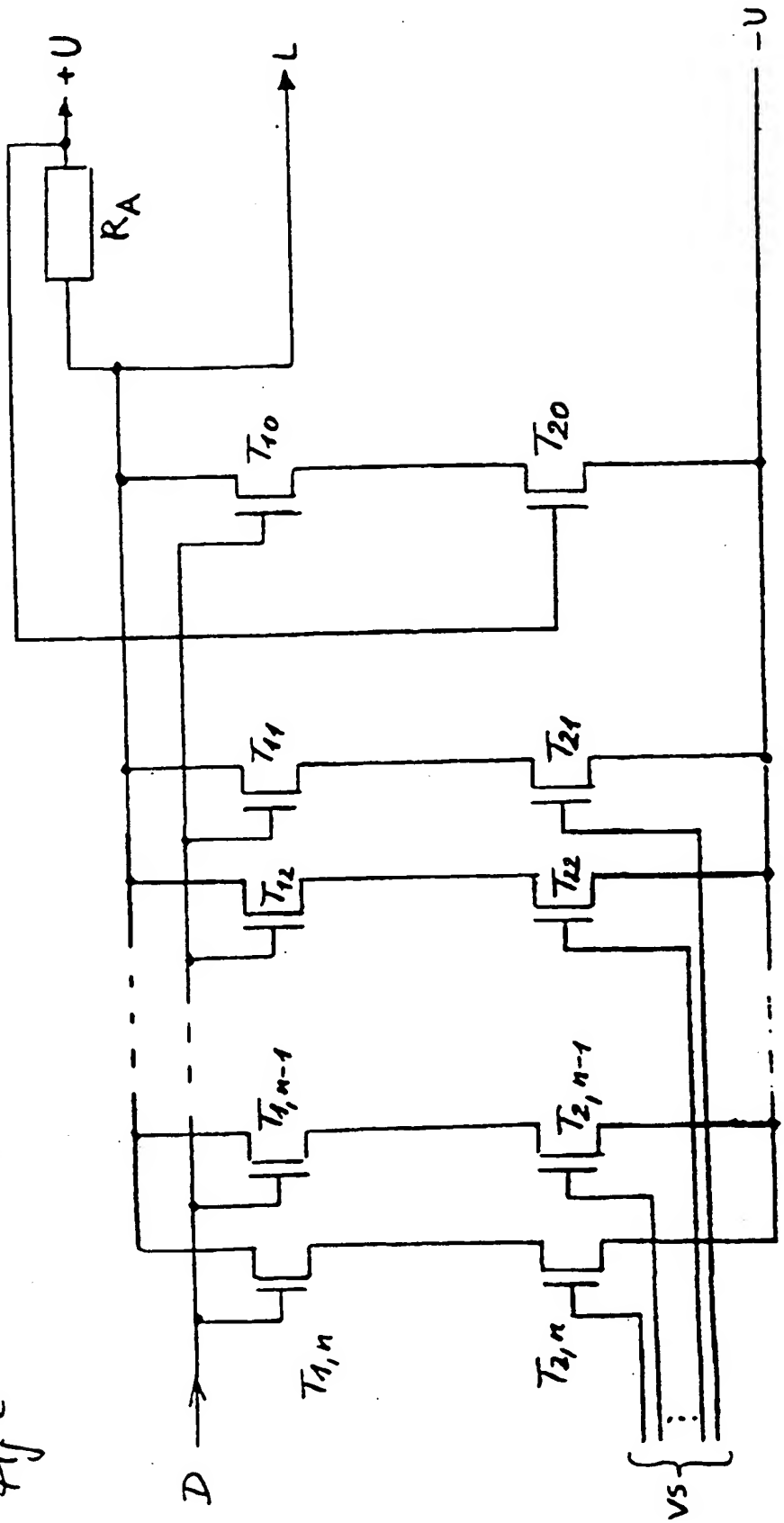
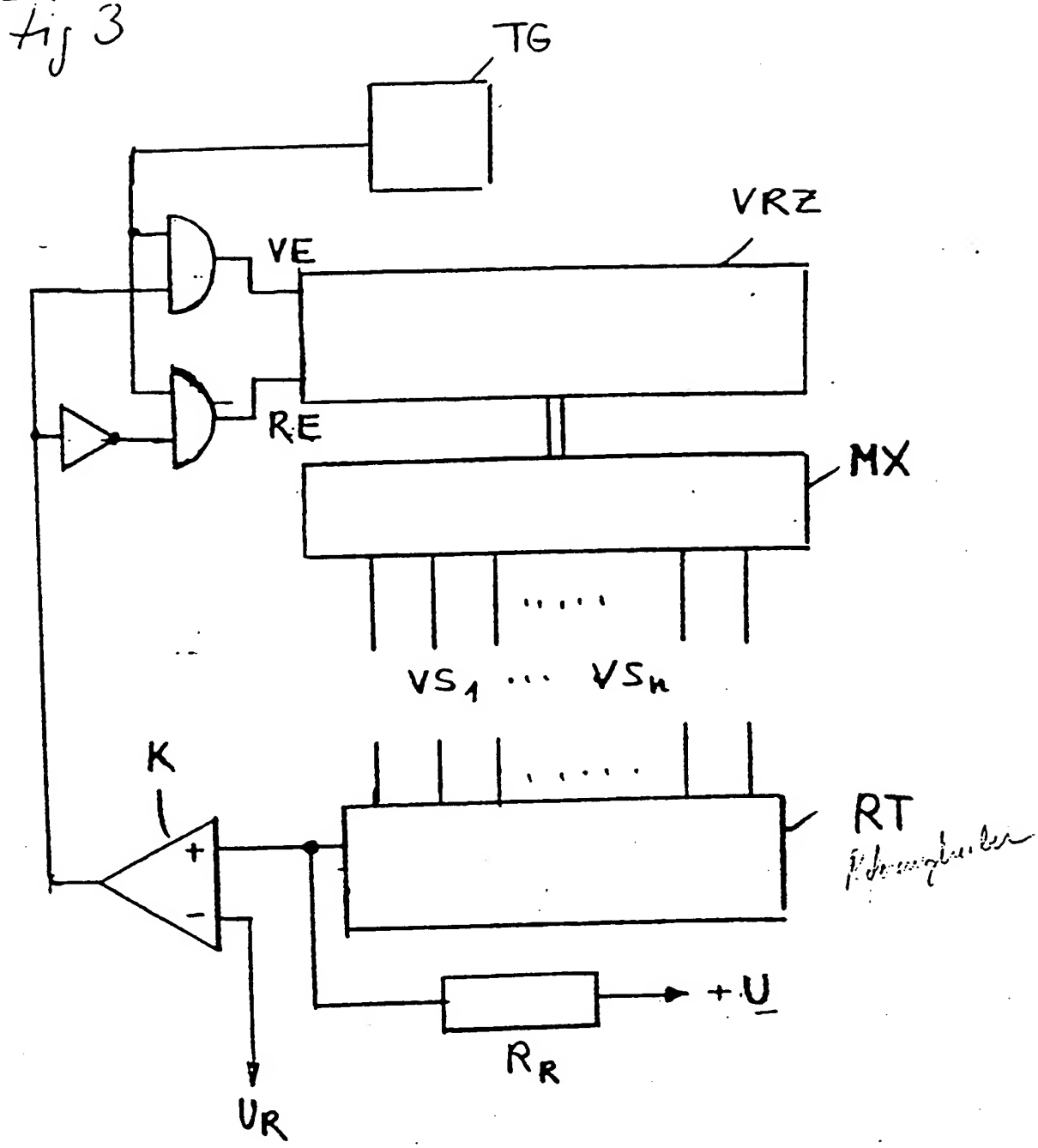



Fig 2

Fig 3



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